UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,582	07/29/2002	Kenneth J. Goodnow	15054	5111

23389 7590 09/30/2004

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
GARDEN CITY, NY 11530

EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,582	GOODNOW ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Figure 2, reference character "30" has been used to designate both error correcting system architecture and clock generator. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- On page 4, line 2 of the paragraph 18 of the specification, "implementing implementing data error checking" is incorrect. It should be --implementing data error checking--.

  Appropriate correction is required.

- On page 5, lines 4-5 of the paragraph 23 of the specification, "error check error check circuit" is incorrect. It should be –error check circuit--.

  Appropriate correction is required.

- On page 6, line 6 of the paragraph 24 of the specification, "error check circuit 30" is incorrect. It should be –error check circuit 33--.

  Appropriate correction is required.

- On page 8, line 11 of the paragraph 29 of the specification, "signals 32" is incorrect. It should be --signals 80--.

  Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 5, 11, 12, 14, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1) in view of Naffziger et al. (US 6,509,788 B2) and Fukazawa (US 6,655,588 B2).

As per claim 1, Sasaki et al. teach a system for dynamically altering a clock speed of a clock signal used for timing of data signal transmissions and receptions within an integrated circuit (IC) device and, means for adjusting said clock speed according to a maximum speed allowed for the IC that avoids said data transmission fail point and data transmissions generated at different clock speeds (page 2, paragraph 15, Sasaki et al.).

However Sasaki et al. do not explicitly teach the specific use of a clock generator circuit for providing said clock signal used for timing of data signal transmission and reception within said IC.

Naffziger et al. in an analogous art teach that the present invention is directed to a system and method, which utilize an on-chip oscillator to provide the appropriate clock frequency for components of the chip to manage power consumption by the chip. More specifically, in a preferred embodiment of the present invention, an on-chip oscillator is utilized to provide the clock frequency for the chip's core circuitry, and such oscillator can dynamically adjust such clock frequency (col. 4, lines 9-16, Naffziger et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Naffziger et al. by including an additional step of using a clock generator circuit for providing said clock signal used for timing of data signal transmission and reception within said IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a clock generator circuit for providing said clock signal used for timing of data signal transmission and reception within said IC would provide the opportunity to use the clock signal to synchronize the operation of different circuit components in the IC.

Sasaki et al. also do not explicitly teach the specific use of a monitoring circuit means for receiving and detecting when a data transmission fail point is achieved.

However Fukazawa in an analogous art teaches that when data is transmitted and received over a signal line between an IC card and a card reader/writer for reading or writing of the data, a data transmitting side transmits a parity based upon content of the data together with the data over the signal line and a data receiving side checks whether or not there is any error in reception of data based upon content of the data and the parity received (col. 5, lines 34-40, Fukazawa).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Fukazawa by including an additional step of using a monitoring circuit means for receiving and detecting when a data transmission fail point is achieved.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a monitoring circuit means for receiving and detecting when a data transmission fail point is achieved would provide the opportunity to change the operational parameters so that the transmitted data is received without any error.

- As per claim 2, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Naffziger et al. teach means for adjusting comprises means for generating a feedback control signal for input to said clock generator circuit for adjusting said clock to said maximum speed (col. 5, lines 14-21, col. 6, lines 18-21, lines 32-33, Naffziger et al.).

- As per claim 5, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Sasaki et al. teach a means for delaying each of a series of data transmission signals generated at different clock speeds; said monitoring circuit comprising including an error check circuit for receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against a corresponding known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission (figure 6, page 2, paragraphs 15-17, Sasaki et al.).

- As per claim 11, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Sasaki et al. teach a method for dynamically altering a system clock speed regulating data signal transmission and receptions in an Integrated Circuit (IC), said method comprising the steps of adjusting said clock speed according to a maximum speed allowed for the IC that avoids said data transmission fail point and receiving data transmissions generated at different clock speeds (page 2, paragraph 15, Sasaki et al.).

Naffziger et al. teach providing said clock signal used for timing of data signal transmission and reception within said IC (col. 4, lines 9-16, Naffziger et al.).

Fukazawa teach detecting when a data transmission fail point is achieved (col. 5, lines 34-40, Fukazawa).

- As per claim 12, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Naffziger et al. teach the method, wherein said adjusting step c) includes the step of generating a feedback control signal for input to said clock generator circuit, said feedback signal for adjusting said clock to said maximum speed (col. 5, lines 14-21, col. 6, lines 18-21, lines 32-33, Naffziger et al.).

- As per claim 14, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Sasaki et al. teach the method, further comprising the steps of: delaying each of a series of data transmission signals generated at different clock speeds; receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against its corresponding

known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission (figure 6, page 2, paragraphs 15-17, Sasaki et al.).

- As per claim 18, Sasaki et al., Naffziger et al. and Fukazawa teach the additional limitations.

Sasaki et al. teach the method, further including the step of continuously detecting presence of data transmission fail points to ensure that the errors do not occur as the IC incurs different operating conditions, said monitoring including adjusting the clock speed accordingly (page 2, paragraph 15, Sasaki et al.).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1), Naffziger et al. (US 6,509,788 B2) and Fukazawa (US 6,655,588 B2) as applied to claim 1 above, and further in view of Li et al. (US 5,477,181).

As per claim 3, Sasaki et al., Naffziger et al. and Fukazawa substantially teach the claimed invention described in claim 1 (as rejected above).

However Sasaki et al., Naffziger et al. and Fukazawa do not explicitly teach the specific use of a clock generator circuit that comprises a multiplexor device comprising one or more clock taps responsive to the feedback control signal for enabling alteration of said clock speed.

Li et al. in an analogous art teach the clock generator that comprises a multiplexor, coupled to said multiphase signal generator, for receiving said plurality of intermediate clock phases and said output control signal and in accordance therewith providing said plurality of additional output clock phases (col. 11, lines 58-63, Li et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Li et al. by including an additional step of using a clock generator circuit that comprises a multiplexor device comprising one or more clock taps responsive to the feedback control signal for enabling alteration of said clock speed.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a clock generator circuit that comprises a multiplexor device comprising one or more clock taps responsive to the feedback control

signal for enabling alteration of said clock speed would provide the opportunity to frequency divide clock signals using the control signal.

7. Claims 4, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1), Naffziger et al. (US 6,509,788 B2) and Fukazawa (US 6,655,588 B2) as applied to claim 2 above, and further in view of Ornes et al. (US 6,748,567 B1).

As per claim 4, Sasaki et al., Naffziger et al. and Fukazawa substantially teach the claimed invention described in claim 2 (as rejected above).

However Sasaki et al., Naffziger et al. and Fukazawa do not explicitly teach the specific use of an error correction signal generating circuit for generating error correction signals according to each data signal transmission, said monitoring circuit comprising including an error correction signal check circuit for receiving said error correction signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error corrections.

Ornes et al. in an analogous art teach an embodiment of a method and system is disclosed that provides a reliable ECC code that is transmitted as part of a serial stream (col. 2, lines 52-54, Ornes et al.). Ornes wt al. also teach that after all of the data to be covered by the ECC code has been communicated to the base code generator 714, the base code generator completes generation of the base ECC code. The resulting 10-bit characters representing the ECC code are communicated to register 710 and finally to FIFO 712, from which they will be serially transmitted (figure 7, col. 8, lines 4-7, lines 22-25, Ornes et al.).

Ornes et al. teach that FIG. 8 shows a receiving system 800 in accordance with an embodiment of the invention. Base code generator generates an expected base ECC code based on the 10-bit data received in the transmitted cell. The base code generator 812 will generate the expected base ECC code in a manner similar to that done by the transmit system, e.g., using the system shown in FIG. 6. Once the transmitted ECC code has been converted back to two 6-bit characters, in one embodiment, then a comparison between the actual transmitted ECC code and the newly generated expected ECC code is made using XOR logic 824. The two codes are bitwise XORed, resulting in a

generated syndrome (every compared bit that does not match will generate a logical "1" and every match will generate a logical "0"). The ECC syndrome indicates, when non-zero, what bit in the data must be flipped to correct a single-bit error. If the ECC syndrome is zero, no error has been detected, and the data will be read from the ECC FIFO without any correction. But if the ECC syndrome is non-zero, correction will be attempted (figure 8, col. 9, lines 13-14, lines 30-34, lines 50-62, Ornes et al.).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Ornes et al. by including an additional step of using an error correction signal generating circuit for generating error correction signals according to each data signal transmission, said monitoring circuit comprising including an error correction signal check circuit for receiving said error correction signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error corrections.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if the transmitted data is received correctly by the receiver and if there is an error in the received data, error correction will be attempted.

- As per claim 13, Sasaki et al., Naffziger et al., Fukazawa and Ornes et al. teach the additional limitations.

Ornes et al. teach the method, further comprising the steps of: generating error correction signals according to each data signal transmission, receiving said error correction signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error corrections (figure 8, col. 9, lines 13-14, lines 30-34, lines 50-62, Ornes et al.).

8. Claims 6-8, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1), Naffziger et al. (US 6,509,788 B2) and Fukazawa (US 6,655,588 B2) as applied to claim 2 above, and further in view of Lambrecht et al. (US 6,775,809 B1).

As per claim 6, Sasaki et al., Naffziger et al. and Fukazawa substantially teach the claimed invention described in claim 2 (as rejected above).

However Sasaki et al., Naffziger et al. and Fukazawa do not explicitly teach the specific use of the system, further comprising: a random data generating circuit for generating unique random data transmission signals for input to said IC device, said IC device for processing said random data in and generating a corresponding data output; said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

Lambrecht et al. in an analogous art teach that referring to FIG. 1, there is shown a typical apparatus for testing the operation of an integrated circuit (IC) memory device 12. The apparatus 10 comprises a vector memory 14 for storing random data sequences. The vector memory 14 is connected to a transmitter 16 for transmitting the random data sequences along a transmission medium 18 to the IC memory device 12. The apparatus 10 also comprises a receiver 20 for receiving data transmitted from the IC memory device 12 via the transmission medium 18, and a result memory 22, connected to the receiver 20, for storing the received data. The operation of the IC memory device 12 is tested by comparing the random data sequences that are transmitted from the vector memory 14 to the IC memory device 12 for storage therein with the same random data sequences after they are transmitted from the IC memory device 12 to the result memory 22 for storage therein. It should be noted that although only one transmitter 16, transmission medium 18, and receiver 20 are shown, this arrangement may be duplicated as required based upon the number of input/output (I/O) lines of the IC memory device 12 to be measured. The apparatus 10 can also be used to attempt to measure the worst case timing and voltage margins of the IC memory device 12 by measuring the output waveforms of the random data sequences

after they are transmitted from the IC memory device 12 to the result memory 22 (figure 1, col. 1, line 50 – col. 2, line 8, Lambrecht et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Lambrecht et al. by including an additional step of using a random data generating circuit for generating unique random data transmission signals for input to said IC device, said IC device for processing said random data in and generating a corresponding data output; said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the operational parameters of the IC device that cause the data transmission failure and change the IC device operational parameters for successful transmission of data.

- As per claim 7, Sasaki et al., Naffziger et al., Fukazawa and Lambrecht et al. teach the additional limitations.

Sasaki et al. teach the system, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit matches said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be increased (page 6, claim 8, Sasaki et al.).

- As per claim 8, Sasaki et al., Naffziger et al., Fukazawa and Lambrecht et al. teach the additional limitations.

Sasaki et al. teach the system, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit does not match said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be decreased (page 6, claim 8, Sasaki et al.).

- As per claim 15, Sasaki et al., Naffziger et al., Fukazawa and Lambrecht et al. teach the additional limitations.

Lambrecht et al. teach the method, further comprising the steps of: generating unique random data transmission signals; transmitting said unique random data signals to said IC device for processing therein, and generating a corresponding data output signal; and, comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output (figure 1, col. 1, line 50 – col. 2, line 8, Lambrecht et al.).

- As per claim 16, Sasaki et al., Naffziger et al., Fukazawa and Lambrecht et al. teach the additional limitations.

Sasaki et al. teach the method, wherein said feedback control signal includes a first signal indicating a match between said data output signal of said data path and said generated unique random data, or generating a second output signal indicating no match between said data output signal of said data path and said generated unique random data, wherein said adjusting step c) includes responding to either said first or second output signals for respectively increasing or decreasing a clock frequency of said clock signal (page 6, claim 8, Sasaki et al.).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1), Naffziger et al. (US 6,509,788 B2), Fukazawa (US 6,655,588 B2) and Lambrecht et al. (US 6,775,809 B1) as applied to claim 6 above, and further in view of Collier (US 2002/0107897 A1).

As per claim 9, Sasaki et al., Naffziger et al., Fukazawa, Lambrecht et al. and Collier substantially teach the claimed invention described in claim 6 (as rejected above).

However Sasaki et al., Naffziger et al., Fukazawa, Lambrecht et al. do not explicitly teach the specific use of the system, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

Collier in an analogous art teaches that when a call for random data is received at input 6 by the random number generator 1 the processing means 2 performs a series of processing steps as described below to generate a random number. The random number is then output by the random number generator at

output 7. When the random number generator is called the processing means is arranged to access a seed value stored in temporary store 5, perform an algorithm which takes the seed value as input and based on that seed value to generate random data and a seed value which is stored for use by the next iteration of the algorithm (figure 1, page 2, paragraph 16, Collier).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Collier by including an additional step of using the system, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate random data that can be used for testing different parameters of a circuit.

10. Claims 10, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. (US 2002/0114224 A1), Naffziger et al. (US 6,509,788 B2) and Fukazawa (US 6,655,588 B2) as applied to claim 5 above, and further in view of Tada et al. (US 2001/0047319 A1).

As per claim 10, Sasaki et al., Naffziger et al., Fukazawa substantially teach the claimed invention described in claim 5 (as rejected above).

However Sasaki et al., Naffziger et al., Fukazawa do not explicitly teach the specific use of the system, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

Tada et al. in an analogous art teach that when a load on a communication line is increased, a delay occurs in operation of a program used by the transmitting server, which delivers data to the receiving servers (page 1, paragraph 8, Tada et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sasaki et al.'s patent with the teachings of Tada et al. by including an additional step of using the system, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the data received by the receiver for errors.

- As per claim 17, Sasaki et al., Naffziger et al., Fukazawa and Tada et al. teach the additional limitations.

Tada et al. teach the method, wherein said delaying step includes the step of increasing a load applied to data lines carrying said data transmission signals to said error check circuit (page 1, paragraph 8, Tada et al.).

Claim Objections

11. Claims 1-18 are objected to because of the following informalities: Claims 1-18 should be indented. Appropriate correction is required.

12. Claim 4 is objected to because of the following informalities: On page 9, line 3 of claim 4; "comprising including" is incorrect. It should be --comprising--. Appropriate correction is required.

13. Claim 5 is objected to because of the following informalities: On page 9, line 3 of claim 5; "comprising including" is incorrect. It should be --comprising--. Appropriate correction is required.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

GUY J. LAMARRE
PRIMARY EXAMINER